

## LOW-VOLTAGE NON-DEGENERATIVE TRANSMITTER CIRCUIT

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BACKGROUND

**[0001]** Complex programmable logic devices (CPLDs) are well-known integrated circuits that may be programmed to perform various logic functions. Numerous types of memory elements may be used in CPLD architectures to provide programmability. One such memory element, known as a flash memory cell, is both electrically programmable and erasable. Program and erase are performed on a plurality of flash memory cells using either Fowler-Nordheim tunneling or hot electron injection for programming and Fowler-Nordheim tunneling for erase. Flash memories can also be in-system programmable (ISP). An ISP device can be programmed, erased, and can have its program state verified after it has been connected, such as by soldering, to a system printed circuit board. Some CPLDs do not have ISP capability and must be programmed externally (outside the system) by programming equipment.

**[0002]** Circuit features grow ever smaller with improvements in integrated-circuit process technology. The reduction in feature size improves device performance while at the same time reducing cost and power consumption. Unfortunately, smaller feature sizes also increase a circuit's vulnerability to over-voltage conditions. Among the more sensitive elements in a modern integrated circuit are the gate oxide layers of the various MOS transistors. In modern devices these layers are very thin, and are consequently easily ruptured by excessive voltage levels. Modern circuits with small feature sizes therefore employ significantly lower source voltages than was common only a few years ago. For example, modern 0.18-micron processes employ supply voltages no greater than 2 volts.

**[0003]** The voltages required to program and erase flash

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memory cells are dictated by physical properties of the materials used to fabricate memory cells. Unfortunately, these physical properties have not allowed the voltages required to program, erase, and verify the program state of a memory cell to be reduced in proportion to reductions in supply voltages. For example, modern flash memory cells adapted for use with a 0.18-micron processes require program and erase voltages as high as 14 volts, a level far exceeding the required supply voltage. Such memory cells are verified using a range of voltages from about zero volts to about 4.5 volts, the upper end of which is also potentially damaging to sensitive circuits. For a more detailed treatment of program, erase, and verify procedures, see U.S. Patent No. 5,889,701, which is incorporated herein by reference.

**[0004]** Figure 1A (prior art) depicts a conventional CPLD 100. CPLD 100 includes a number of input/output (I/O) circuits 105 that may be configured as either input circuits or output circuits by programming appropriate ones of a collection of memory cells 110. Memory cells 110 are depicted in a box for simplicity: they are typically distributed throughout CPLD 100. CPLD 100 includes many additional functional components that are omitted here for brevity. For a more detailed discussion of exemplary CPLDs, see U.S. Patent No. 6,288,526 and "CoolRunner® XPLA3 CPLD, Advance Product Specification," DS012 (v1.4), April 11, 2001, both of which are incorporated herein by reference.

**[0005]** I/O circuits 105 are externally accessible via a number of device I/O pins 115. Pins 115 are used both when CPLD 100 is operating as a programmed logic circuit (i.e., is in a logic mode) and during program and verify procedures performed when CPLD 100 is in the test mode. A power line 120 conveys a power-supply voltage VDD from an external supply pin 122 to I/O circuits 105 and the other logic circuits (not shown). CPLD 100 may also include internal voltage generators for developing relatively high voltages to support ISP functionality.

**[0006]** The I/O circuit 105 in the upper left-hand corner of CPLD 120 is shown to include a device input circuit 125 connected to supply line 120. Input circuit 125 has a device input terminal adapted to receive input signals from one of device pins 115 and an output terminal 135 adapted to convey signals to internal logic (not shown). Each I/O circuit 105 also includes an output circuit 130 adapted to convey signals from the internal logic to the respective device pin 115.

**[0007]** During program-state verification, an analog verification signal VFY of between about 0 and 4.5 volts is applied to the control gates of various ones of memory cells 110 via a transmitter circuit 145 and some steering logic 140. As with other designations in the present disclosure, VFY refers to both the verification signal and the corresponding circuit node. Whether a given designation refers to a node or a signal will be clear from the context.

**[0008]** A high-voltage signal HVIN activates transmitter circuit 145 when brought high to pass the verify signal VFY to steering logic 140. As explained below in connection with Figure 1B, high-voltage signal HVIN is even higher than the maximum verify voltage VFY, and consequently approaches a level that might damage circuits -- such as delicate gate oxides -- internal to input circuit 125. High-voltage signal HVIN is therefore brought onto CPLD 100 via a dedicated pin 120.

**[0009]** Figure 1B details transmitter circuit 145 of Figure 1A, including a level shifter 150 and an NMOS output transistor 155. Level shifter 150 shifts a digital control signal CTRL that varies between zero volts and VDD to a similar control signal HV that varies between zero volts and the verify voltage VFY. Control signal CTRL turns off the switched VFY signal VFY\_S while steering logic 140 selects the next bit line to which the verify signal VFY will be applied.

**[0010]** Due to the threshold voltage  $V_{th}$  of transistor 155, verify voltage VFY\_S will be less than the externally applied

verify voltage VFY unless the gate of transistor 155 is brought well above verify voltage VFY. Verify voltage VFY may exceed VDD, and the voltage applied to the gate of transistor 155 must be higher still.

**[0011]** Unfortunately, input circuits 125 in state-of-the-art CPLDs may contain device features too small to accommodate the relatively high voltage HVIN required on device pin 120. For example, if I/O circuits 105 are manufactured using a conventional 0.18-micron process, voltages over about 5 volts can damage input transistors within input circuit 125. The maximum verify voltages VFY required for memory cells 110 in such circuits is approximately 4.5 volts, so verify voltages VFY can be connected to the input terminal of input circuit 125 as shown; however, the threshold voltage required to pass a 4.5 volt signal through transistor 145 without substantial degradation will be approximately 6 or 7 volts. A dedicated device pin 120 is therefore provided to convey this relatively high voltage HUIN.

**[0012]** Integrated circuits are becoming ever more densely populated as processing technology improves. As circuit features grow smaller, the number of physical pads that fit on the die surface becomes a limiting factor on the amount of logic instantiated on a circuit die. Due to the pad-limited nature of modern devices, device pins are at a premium. It is therefore undesirable to provide a dedicated pin 120 for the purposes of test at the expense of a general purpose I/O circuit 105.

#### SUMMARY

**[0013]** A CPLD in accordance with the invention employs a low-voltage, non-degenerative transmitter circuit to eliminate the need for a dedicated control pin to provide the relatively high voltage levels required to verify the program states of programmable memory cells. Eliminating the need for a dedicated control pin frees up valuable chip real

estate for the inclusion of an additional general-purpose input/output pin.

**[0014]** The appended claims, and not this summary, define the scope of the invention.

#### BRIEF DESCRIPTION OF THE FIGURES

**[0015]** Figure 1A (prior art) depicts a conventional CPLD 100.

**[0016]** Figure 1B details transmitter circuit 145 of Figure 1A, including a level shifter 150 and an NMOS output transistors 155.

**[0017]** Figure 2 depicts a CPLD 200 in accordance with one embodiment of the invention.

**[0018]** Figure 3 depicts a transmitter circuit 300 that may be used in place of transmitter circuit 205 of Figure 2.

**[0019]** Figure 4 depicts an embodiment of switch section 305 of Figure 3.

**[0020]** Figure 5 depicts an embodiment of switch section 310 of Figure 3.

#### DETAILED DESCRIPTION

**[0021]** Figure 2 depicts a CPLD 200 similar to CPLD 100 of Figure 1, like numbered elements being the same. In accordance with the invention, transmitter circuit 145 is replaced with a transmitter circuit 205 that eliminates the need for a dedicated pin to provide the voltage HUIN while verifying the program states of memory cells 110. Transmitter circuit 205 includes a transistor 210 that gates verify voltage VFY to steering logic 140. Circuit 205 also includes an amplifier 215 that uses verify voltage VFY to develop a relatively high voltage on the gate of transistor 210, thereby enabling transistor 210 to convey verify voltage VFY to steering logic 140 without a significant voltage drop.

**[0022]** Figure 3 depicts a transmitter circuit 300 that may be used in place of transmitter circuit 205 of Figure 2 in

one embodiment of the invention. Circuit 300 includes a first switch section 305 and a second switch section 310.

**[0023]** The first switch section 305 is adapted to pass verify voltage VFY when VFY is greater than supply voltage VDD, while the second switch section 310 is adapted to pass verify voltage VFY when VFY is less than or equal to supply voltage VDD.

**[0024]** In addition to verify voltage VFY, circuit 300 receives a clock signal CLK and a control signal CTRL. These signals can be provided externally via conventionally I/O circuits, or can be developed using logic internal to CPLD 200. Circuit 300 uses these three input signals, as detailed below in connection with Figures 4 and 5, to develop a controlled verify voltage VFY\_S for verifying the program states of memory cells 110 (Figure 2). Inverted versions of signals CLK and CTRL, CLKB and CTRLB, pass from switch section 305 to switch section 310 for reasons that will be evident from the following discussion.

**[0025]** Figure 4 depicts an embodiment of switch section 305 of Figure 3. Switch section 305 includes a NAND gate 410, a level shifter 415, a voltage doubler 420, an output stage 425, and an enable circuit 430. Setting control terminal CTRL to logic one enables switch stage 305. NAND Gate 410 then passes an inverted version of signal CLK to level shifter 415.

**[0026]** During operation, the test voltage VFY can vary between about zero volts and a level well above VDD. The clock and enable signals, on the other hand, are derived from VDD; consequently, level shifter 415 is used to level shift clock signal CLK. The resulting level-shifted clock SCLK and its complement SCLKB are passed to voltage doubler 420. Voltage doubler 420, an amplifier that provides an output voltage greater than its supply voltage, uses these clock signals as inputs, and verify voltage VFY as a supply voltage, to produce a pair of high-voltage signals HV1 and HV2 to the gates of respective transistors 435 and 440 of

output circuit 425. High voltage signals HV1 and HV2 are approximately twice verify voltage VFY, and are therefore sufficiently high that transistors 435 and 440 pass verify voltage VFY as verify voltage VFY\_S without appreciable voltage degradation.

**[0027]** Returning control signal CTRL to logic zero removes the clock signal from the input of level shifter 415 and causes enable circuit 430 to pull the gates of transistors 435 and 440 to ground, thereby disconnecting verify voltage terminal VFY from output terminal VFY\_S. Enable circuit 430 produces an inverted version of control signal CTRL, CTRLB, for switch section 310.

**[0028]** Figure 5 depicts an embodiment of switch section 310 of Figure 3, which passes verify voltage VFY when verify voltage VFY is less than or equal to the supply voltage VDD. Switch section 310 includes a voltage doubler 500, an output stage 510, and an enable circuit 515. Voltage doubler 500 is powered by supply voltage VDD, which is sufficiently high to pass verify voltage VFY when verify voltage VFY is below VDD. Other than the supply voltage, voltage doubler 500 works in the same manner as voltage doubler 420 of Figure 4 to produce a pair of high-voltage signals HV3 and HV4 to a pair of transistors 520 and 525 in output stage 510. Signals HV3 and HV4 are sufficiently high to allow transistors 520 and 525 to pass verify voltage VFY to terminal VFY\_S without an appreciable voltage drop.

**[0029]** When the verify mode is no longer selected, or when steering logic 140 is to select a different memory cell, the control terminal CTRL (Figures 3 and 4) is pulled low, causing terminal CTRLB of Figure 5 to go high. Enable circuit 515 consequently pulls the gates of transistors 520 and 525 to ground. Grounding the gates of the transistors in output circuit 510 disconnects terminal VFY from output terminal VFY\_S, thereby making the associated I/O circuit 105 (Figure 2) available during device operation.

**[0030]** In one embodiment, supply voltage VDD is 1.8 volts

and verify voltage VFY can be adjusted anywhere between 0 volts and 4.5 volts. Switch section 305 cannot pass voltages on the lower end of the verify-voltage spectrum, as switch section 305 uses the verify voltage as its supply voltage. In contrast, switch section 310 is supplied by VDD, and consequently cannot pass voltages on the higher end of the verify voltage spectrum. The two switch sections 305 and 310 are therefore connected in parallel so that their combined functionality allows verify voltage VFY to be accurately reproduced at terminal VFY\_S regardless of the level of verify voltage VFY.

**[0031]** While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. For example, application of the invention is not limited to the above-described CPLD architecture, or even to CPLDs. Moreover, some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance, the method of interconnection establishes some desired electrical communication between two or more circuit nodes or terminals. Such communication may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.